ABSTRACT OF THE DISCLOSURE

A logic simulation apparatus is provided with a circuit dividing unit (6) that selects and defines logic cones each of which carries out a logic operation in synchronization with one clock domain as target portions to be speeded up from logic cones extracted by a logic cone extracting unit (5), and that defines logic cons each of which carries out a logic operation based on a plurality of clock domains as nontarget portions not to be speeded up, and a logic compressing unit (7) that compresses the logic of each of the target portions, and performs a logic simulation on each of the target portions whose logic is compressed and also on performs a logic simulation on each of the nontarget portions.